

FIG. 3a

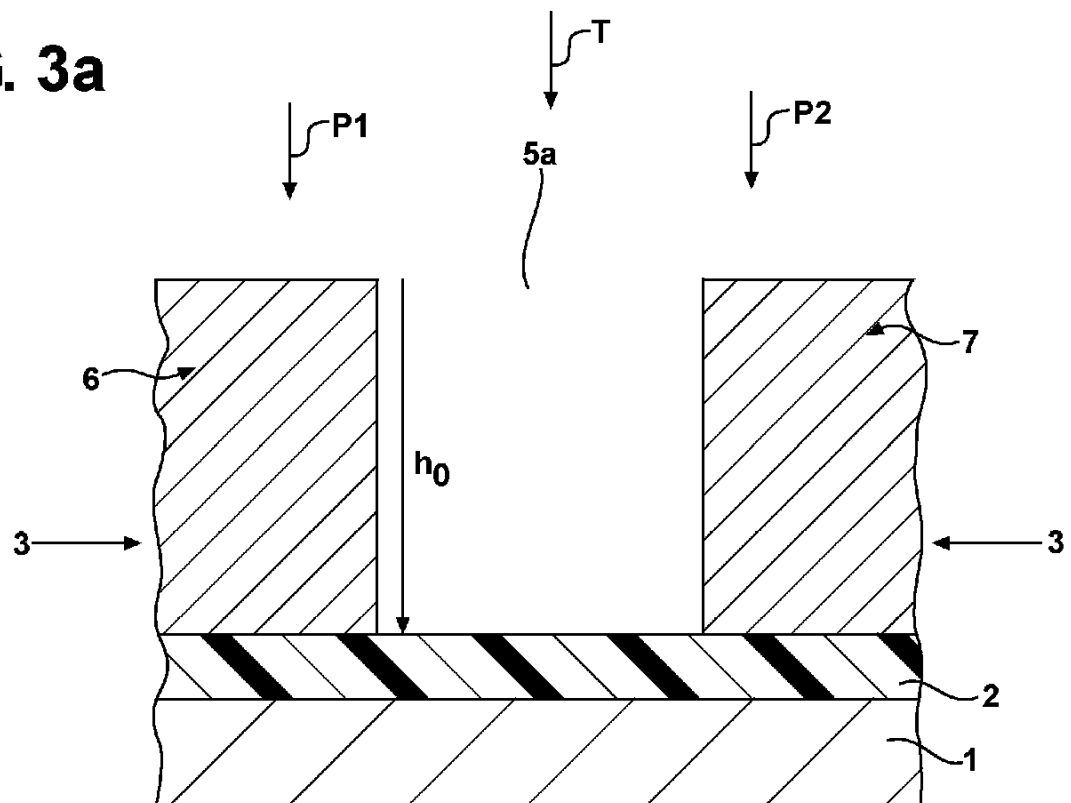
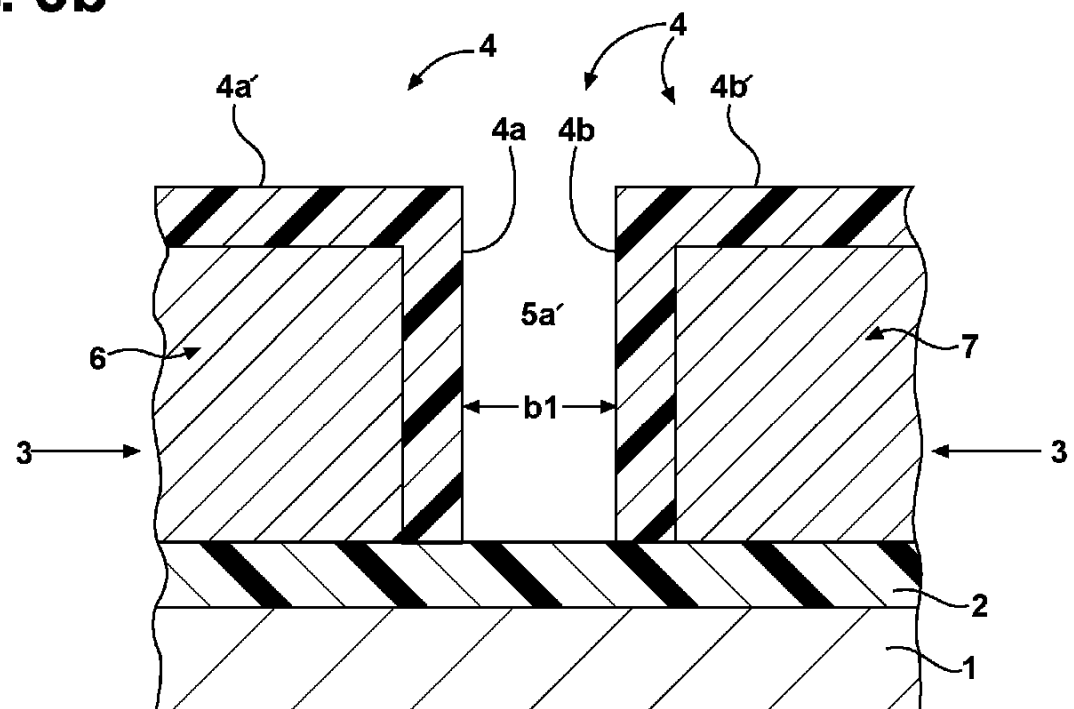


FIG. 3b



A cross-sectional view of a semiconductor device. A central layer 5 is shown with a sub-layer 5* below it. The height of layer 5 is indicated by h_7 and the height of layer 5* is indicated by h_8 . The device is surrounded by a material 6, which is in turn surrounded by a material 7. A dashed line 4c is shown at the top, and a solid line 4a is shown at the bottom. A hatched region 4b is at the bottom, and a hatched region 4b' is at the top. A hatched region 4d is on the right. A hatched region 4a' is on the left. A hatched region 4b is at the bottom, and a hatched region 4b' is at the top. A hatched region 4d is on the right. A hatched region 4a' is on the left. A hatched region 4b is at the bottom, and a hatched region 4b' is at the top. A hatched region 4d is on the right. A hatched region 4a' is on the left.

4/5

FIG. 3e

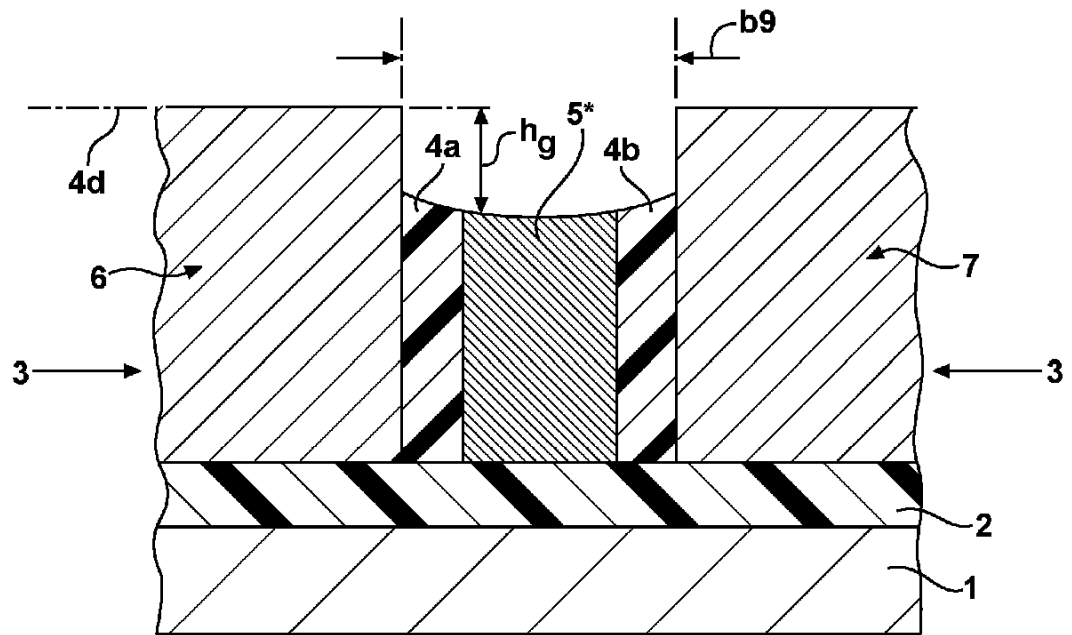
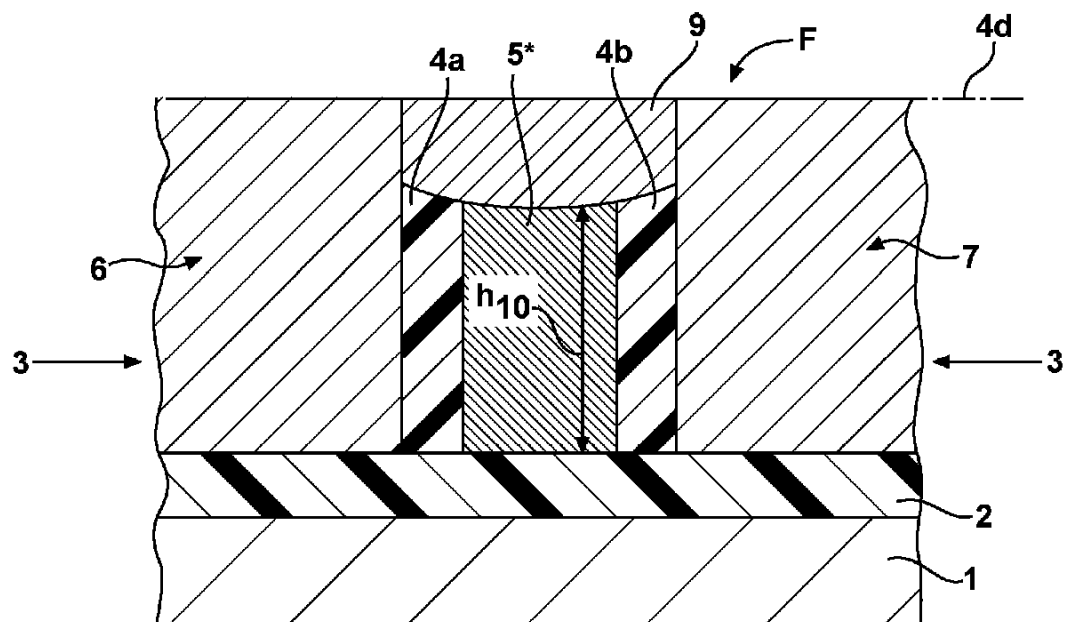


FIG. 3f



5/5

FIG. 4

